active semiconductor layer by a barrier layer provided between them, or by an insulating barrier layer in the case of a conducting conversion layer. Thin layers may be applied to surfaces to aid in maintaining the aforementioned intimate contacts.

Please replace paragraph [0028] with the following amended paragraph:

[0028] This application hereby incorporates by reference the application entitled "Semiconductor Substrate Incorporating a Neutron Conversion Layer", ~~assigned NC 84,785,~~ filed on date even herewith, now issued at U.S. Patent No. 6,867,444. The present invention is directed to a neutron detection device that utilizes a neutron conversion layer in close proximity to charge-sensitive elements such as conventional memory cells. Specifically, the device provides a neutron conversion layer in close proximity to the active semiconductor layer of a charge-sensitive electronic semiconductor device such as a semiconductor memory cell. In particular, the invention will be described with reference to an SRAM memory device formed on a SOI substrate. It will be understood, however, that the invention is not limited to the specifically disclosed embodiment disclosed with reference to silicon devices but may also be realized with other semiconductor materials, and that alpha-emitting neutron converters based on boron and lithium may be utilized as may other alpha emitters, proton emitters, or electron emitters, and may also be utilized with other charge-sensitive device structures such as dynamic random access memories (DRAMs), other types of random access memories, non-random access memories, charge coupled devices, charge injection devices, or other memory device structures and substrates.

Please replace paragraph [0029] with the following amended paragraph:

[0029] FIG. 1 illustrates a conventional SRAM memory device formed on a SOI substrate. The SOI substrate 10 includes an active semiconductor layer 12, an insulating layer 14 (referred to as a buried oxide "BOX") and a base substrate 16. As will be readily understood by those skilled in the art, active charge-sensitive circuit elements such as individual memory cells ~~15~~ are formed in part by modifications made within the active semiconductor layer ~~14~~ 12 of the SOI substrate 10. Additional structural layers are then formed over the active semiconductor layer ~~14~~ 12

to form the working circuitry and circuit elements of the charge-sensitive device. The additional structural layers, for example, may include interconnect layers, insulating layers and/or additional circuit elements. In FIG. 1, these additional structural layers are not illustrated in detail for the sake of simplicity of illustration, but will simply be shown as a single circuit structure layer 18. It is noted, however, that the thickness of the additional structural layers that form the circuit structure layer 18 is generally much greater than the active semiconductor layer 12 or in the insulating layer 14. It is also common to include a passivation layer 20 on top of the circuit structure layer 18.

Please replace paragraph [0030] with the following amended paragraph:

[0030] Previous attempts at utilizing conventional memory devices have concentrated on coating a neutron conversion layer on top of the passivation layer 20 or on removing the passivation layer 20 and coating the neutron conversion layer on top of the circuit structure layer 18. However. the range of alpha particles emitted from a reaction between neutrons and a neutron conversion material (for example the isotope boron-10) is limited. The conventional attempts essentially placed the neutron conversion layer ~~to~~ too far from the active semiconductor layer 12, i.e., beyond the range of the alpha particles resulting in poor sensitivity. Instead. the present invention places a neutron conversion layer in close proximity (either directly in contact with or effectively adjacent to as will be described) to the active semiconductor layer 12 without disrupting or damaging the additional structural layers provided in the circuit structure layer 18, as will be described below.

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Please replace paragraph [0032] with the following amended paragraph:

[0032] Once the base substrate 16 has been substantially removed, a neutron conversion layer 24 is applied to the exposed insulating layer 14 as shown in FIG. 3. Sputter coating will produce lower thermal stresses in the circuit structure layer ~~48~~ 18 during the deposition process, and, for fragile circuits. is therefore over. for example. high temperature processing. Prior to the application of the neutron conversion layer 24, a barrier layer 26 (for an example silicon nitride) may be deposited to prevent diffusion of the neutron conversion material into the active semiconductor layer 12. This process insures that the neutron conversion layer 24 is located in close

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proximity to the active semiconductor layer 12. If desired, an additional stability layer (not shown) such as epoxy may be applied to an outer layer if needed for additional mechanical stability.

Please replace paragraph [0034] with the following amended paragraph:

[0034] Boron containing layers, however, have also been placed directly on silicon diodes. McGregor et al. (cited above) have shown that mechanically stable films of the required thickness can be achieved if provision for stress relief is included. It is well known that ~~borosilicate~~ borophosphosilicate glass ~~(BSPG)~~ (BPSG) is compatible with application on silicon devices, is an insulator, and is commonly used for passivation layers. A ~~BSPG~~ BPSG with 5% boron to serve as the insulating layer 14 and also the neutron conversion layer 24 may also be applied directly to the active semiconductor layer 12 as shown in FIG. 4. Other Boron compounds or compositions may also be used.

Please replace paragraph [0036] with the following amended paragraph:

[0036] The susceptibility of memory devices to SEU in general has been extensively studied for many years, and has revealed an important quantity called the critical charge (Qcrit). The Qcrit is the amount of charge a memory cell must accumulate in order to produce a bit error. It has long been known that finer lithographic line widths lead to smaller cells, to smaller cell charge holding capacity, and thus to smaller Qcrit for higher density memory devices. A graph illustrating the Qcrit for unhardened silicon memory cells based on feature size is shown in FIG. 7. By locating the neutron conversion layer ~~18~~ 24 in close proximity to the active semiconductor layer 12 in which memory cell elements are formed, sufficient charge can be generated by the alpha particles produced by the interaction of the neutrons with the boron-10.

Please replace paragraph [0037] with the following amended paragraph:

[0037] In the case of the device illustrated in FIG. 3, the typical 200 nm thickness of the active semiconductor layer 12 is much less than the range of the alpha particles generated in the neutron conversion layer 24. While the alpha will now reach the active semiconductor layer as

required, only a fraction of the alpha energy will therefore be deposited in the active semiconductor layer 12 as it passes through that layer. The relevant quantity then becomes the amount of energy deposited along the track of the alpha particles, i.e., the Linear Energy Transfer (LET). The LET of an alpha particle from boron-10 traversing silicon is plotted in FIG. 8. (The initial energy of an alpha particle emitted by a boron-10 atom is approximately one and a half MeV.) It can be seen that the LET varies from about 1 to 1.5 ~~Mev~~ MeV/(mg cm^2) over essentially the entire useful energy range of the alpha particle. Applying these limits to a 200 nm active semiconductor layer thickness gives a range of energy deposited in the active semiconductor layer 12 for normal incidence (the charge will increase for non-normal incidence with greater path lengths through the active silicon layer 12). From this range of deposited alpha energy (in MeV) the corresponding amount of charge (in pC) liberated in the active semiconductor layer can be calculated. ~~The amount of alpha energy required (in MeV) per liberated charge (in pC) can be calculated.~~ See "Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices". E. L. Peterson et al., IEEE Transactions on Nuclear Science, NS-29/6, December 1982. 2055-63, the contents of which are incorporated herein by reference. For the illustrated example, the energy is 22.5 MeV/pC giving a value of about 2 to 3 femtocouloubs deposited in the active layer at normal incidence.

Please replace paragraph [0038] with the following amended paragraph:

[0038] FIG. 7 can now be plotted as shown in FIG. 9 to include these limiting values for liberating charge in the active semiconductor layer. As shown in FIG. 9, the alpha particle produced will--at almost any point in its trajectory in silicon--supply an amount of charge comparable to Qcrit for a 0.35 micron line width SOI RAM cell. In other words, the proximally placed neutron conversion layer 24 will produce alpha particles sufficient to cause SEU in conventional SOI RAM structures. The resulting structure will be referred to as a neutron sensitive random access memory ~~(NRAM)~~.

Please add the following new paragraph after paragraph [0030]: